

1 CLAIMS:

2 1. A method of incorporating nitrogen into a silicon-oxide-  
3 containing layer, comprising:

4 exposing the silicon-oxide-containing layer to activated nitrogen  
5 species from a nitrogen-containing plasma to introduce nitrogen into the  
6 layer; the layer being maintained at less than or equal to 400°C during  
7 the exposing; and

8 thermally annealing the nitrogen within the layer to bond at least  
9 some of the nitrogen to silicon proximate the nitrogen.  
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11 2. The method of claim 1 wherein the layer is maintained at  
12 a temperature of from 50°C to 400°C during the exposing.  
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14 3. The method of claim 1 wherein the plasma is maintained  
15 with a power of from about 500 watts to about 5000 watts during the  
16 exposing.  
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18 4. The method of claim 1 wherein the plasma is maintained  
19 with a power of from about 500 watts to about 3000 watts during the  
20 exposing.  
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1           5.     The method of claim 1 wherein the exposing occurs within  
2 a reactor, and wherein a pressure within the reactor is from about  
3 5 mTorr to about 10 mTorr during the exposing.  
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5           6.     The method of claim 1 wherein the exposing occurs for a  
6 time of less than or equal to about 1 minute.  
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8           7.     The method of claim 1 wherein the exposing occurs for a  
9 time of from about 3 seconds to about 1 minute.  
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11          8.     The method of claim 1 wherein the exposing occurs for a  
12 time of from about 10 seconds to about 15 seconds.  
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14          9.     The method of claim 1 wherein the annealing comprises  
15 rapid thermal processing at a ramp rate of at least about 50°C/sec to  
16 a temperature of less than 1000°C, with such temperature being  
17 maintained for at least about 30 seconds.  
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19          10.    The method of claim 1 wherein the annealing comprises  
20 thermal processing at temperature of less than 1100°C for a time of at  
21 least 3 seconds.  
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1 11. A method of forming a nitrogen-enriched region within a  
2 silicon-oxide-containing layer, comprising:

3 providing the silicon-oxide-containing layer over a substrate; the  
4 layer having an upper surface above the substrate and a lower surface  
5 on the substrate;

6 exposing the layer to activated nitrogen species from a nitrogen-  
7 containing plasma to introduce nitrogen into the layer and form a  
8 nitrogen-enriched region, the nitrogen enriched region being only in an  
9 upper half of the silicon-oxide-containing layer; and

10 thermally annealing the nitrogen within the nitrogen-enriched region  
11 to bond at least some of the nitrogen to silicon proximate the nitrogen;  
12 the nitrogen-enriched region remaining confined to the upper half of the  
13 silicon-oxide-containing layer during the annealing; the thermal annealing  
14 comprising either (1) thermal processing at a temperature of less than  
15 1100°C for a time of at least 3 seconds, or (2) rapid thermal processing  
16 at a ramp rate of at least about 50°C/sec to a process temperature of  
17 less than 1000°C, with the process temperature being maintained for at  
18 least about 30 seconds.

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20 12. The method of claim 11 wherein the nitrogen-enriched region  
21 is formed only in the upper third of the silicon-oxide layer by the  
22 exposing.  
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13. The method of claim 11 wherein the nitrogen-enriched region is formed only in the upper third of the silicon-oxide layer by the exposing and remains confined to the upper third of the silicon-oxide containing layer during the annealing.

14. The method of claim 11 wherein the nitrogen-enriched region is formed only in the upper fourth of the silicon-oxide layer by the exposing and remains confined to the upper fourth of the silicon-oxide containing layer during the annealing.

15. The method of claim 11 wherein the nitrogen-enriched region is formed only in the upper fifth of the silicon-oxide layer by the exposing and remains confined to the upper fifth of the silicon-oxide containing layer during the annealing.

16. The method of claim 11 wherein the layer is maintained at a temperature of less than 400°C during the exposing.

17. The method of claim 11 wherein the plasma is maintained with a power of from about 500 watts to about 5000 watts during the exposing.

1           18. The method of claim 11 wherein the exposing occurs within  
2 a reactor, and wherein a pressure within the reactor is from about  
3 5 mTorr to about 10 mTorr during the exposing.

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5           19. The method of claim 11 wherein the exposing occurs for a  
6 time of less than or equal to about 1 minute.

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8           20. A method of forming a transistor, comprising:  
9 forming a gate oxide layer over a semiconductive substrate, the  
10 gate oxide layer comprising silicon dioxide;  
11 exposing the gate oxide layer to activated nitrogen species from a  
12 nitrogen-containing plasma to introduce nitrogen into the layer, the layer  
13 being maintained at less than or equal to 400°C during the exposing;  
14 thermally annealing the nitrogen within the layer to bond at least  
15 a majority of the nitrogen to silicon proximate the nitrogen;  
16 forming at least one conductive layer over the gate oxide; and  
17 forming source/drain regions within the semiconductive substrate;  
18 the source/drain regions being gatedly connected to one another by the  
19 conductive layer.

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21           21. The method of claim 20 wherein the conductive layer is  
22 formed on the gate oxide.  
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1           22. The method of claim 20 wherein the conductive layer is  
2 formed after the annealing.

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4           23. The method of claim 20 wherein the source/drain regions are  
5 formed after the annealing.

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7           24. The method of claim 20 wherein the conductive layer and  
8 source/drain regions are formed after the annealing.

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10          25. The method of claim 20 wherein the plasma is maintained  
11 with a power of from about 500 watts to about 5000 watts during the  
12 exposing.

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14          26. The method of claim 20 wherein the exposing occurs within  
15 a reactor, and wherein a pressure within the reactor is from about  
16 5 mTorr to about 10 mTorr during the exposing.

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18          27. The method of claim 20 wherein the exposing occurs for a  
19 time of less than or equal to about 1 minute.  
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1           28. The method of claim 20 wherein the annealing comprises  
2 thermal processing at temperature of less than 1100°C for a time of at  
3 least 3 seconds.

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5           29. A method of forming a transistor, comprising:  
6 forming a gate oxide layer over a semiconductive substrate, the  
7 gate oxide layer comprising silicon dioxide; the gate oxide layer having  
8 an upper surface and a lower surface;

9 exposing the gate oxide layer to activated nitrogen species from a  
10 nitrogen-containing plasma to introduce nitrogen into the gate oxide layer  
11 and form a nitrogen-enriched region, the nitrogen enriched region being  
12 only in an upper half of the gate oxide layer;

13 thermally annealing the nitrogen within the nitrogen-enriched region  
14 to bond at least a majority of the nitrogen to silicon proximate the  
15 nitrogen; the nitrogen-enriched region remaining confined to the upper  
16 half of the silicon-oxide-containing layer during the annealing;

17 forming at least one conductive layer over the gate oxide layer;  
18 and

19 forming source/drain regions within the semiconductive substrate;  
20 the source/drain regions being gatedly connected to one another by the  
21 conductive layer.  
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1           30. The method of claim 29 wherein the nitrogen-enriched region  
2 is formed only in the upper third of the silicon-oxide layer by the  
3 exposing.

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5           31. The method of claim 29 wherein the nitrogen-enriched region  
6 is formed only in the upper third of the silicon-oxide layer by the  
7 exposing and remains confined to the upper third of the silicon-oxide  
8 containing layer during the annealing.

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10          32. The method of claim 29 wherein the layer is maintained at  
11 a temperature of less than 400°C during the exposing.

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13          33. The method of claim 29 wherein the plasma is maintained  
14 with a power of from about 500 watts to about 5000 watts during the  
15 exposing.

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17          34. The method of claim 29 wherein the exposing occurs within  
18 a reactor, and wherein a pressure within the reactor is from about  
19 5 mTorr to about 10 mTorr during the exposing.

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21          35. The method of claim 29 wherein the exposing occurs for a  
22 time of less than or equal to about 1 minute.  
23



1           36. The method of claim 29 wherein the annealing comprises  
2 thermal processing at temperature of less than 1100°C for a time of at  
3 least 3 seconds.

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5           37. The method of claim 29 wherein the conductive layer is  
6 formed on the gate oxide.

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8           38. The method of claim 29 wherein the conductive layer is  
9 formed after the annealing.

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11           39. The method of claim 29 wherein the source/drain regions are  
12 formed after the annealing.

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14           40. The method of claim 29 wherein the conductive layer and  
15 source/drain regions are formed after the annealing.

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41. A transistor structure, comprising:

a gate oxide layer over a semiconductive substrate, the gate oxide layer comprising silicon dioxide; the gate oxide layer having a nitrogen-enriched region which is only in an upper half of the gate oxide layer;

at least one conductive layer over the gate oxide layer; and

source/drain regions within the semiconductive substrate; the source/drain regions being gately connected to one another by the conductive layer.

42. The structure of claim 41 wherein the conductive layer comprises conductively-doped silicon.

43. The structure of claim 41 wherein the conductive layer comprises p-type conductively-doped silicon.

44. The structure of claim 41 wherein the nitrogen-enriched region is only in the upper third of the gate oxide layer.

45. The structure of claim 41 wherein the nitrogen-enriched region is only in the upper fourth of the gate oxide layer.

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46. The structure of claim 41 wherein the nitrogen-enriched region is only in the upper fifth of the gate oxide layer.

47. The structure of claim 41 wherein the gate oxide layer is at least about 5Å thick, and wherein the nitrogen-enriched region is only in the upper 50% of the gate oxide layer.